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Date: 5/27/03

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# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

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|---|---|---|---|
| Applicant(s): | Jeffrey A. Shields, *et al.* | Examiner: | Joannie A. Garcia |
| Serial No: | 09/728,554 | Art Unit: | 2823 |
| Filing Date: | December 1, 2000 | | |

Title: DUAL SPACER PROCESS FOR NON-VOLATILE MEMORY DEVICES

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**Commissioner for Patents**
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## APPEAL BRIEF

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Dear Sir:

Applicants submit this brief in triplicate in connection with an appeal of the above-identified patent application. The Commissioner is authorized to deduct $320.00 for the fee associated with this brief from Deposit Account No. 50-1063.

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## I. Real Party in Interest (37 C.F.R. § 1.192(c)(1))

The real party in interest in the present appeal is Advanced Micro Devices, Inc., the assignee of the present application.

## II. Related Appeals and Interferences (37 C.F.R. § 1.192(c)(2))

Appellants, appellants' legal representatives, and/or the assignee of the present application are not aware of any appeals or interferences which will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

## III. Status of Claims (37 C.F.R. § 1.192(c)(3))

Claims 1, 2, and 5-14 are pending in the application. The rejection of claims 1, 2, and 5-14 is appealed.

## IV. Status of Amendments (37 C.F.R. § 1.192(c)(4))

No claim amendments have been made subsequent to the final rejection of December 31, 2002.

## V. Summary of Invention (37 C.F.R. § 1.192(c)(5))

A method of fabricating dual insulating spacers located adjacent to plural polysilicon lines in each of a nonvolatile memory cell and its peripheral circuitry is disclosed in the subject application. (p.6, ll. 1-9). In particular, the method involves depositing a first oxide layer over at least two adjacent polysilicon lines in each of a core area and a periphery area (p. 5, ll. 25-27); implanting an area located between at least two adjacent polysilicon lines in the core area (p. 6, ll. 2-3; p. 7, ll. 1-2), wherein the core area retains an amount of the second oxide between the adjacent polysilicon lines (p. 7, ll. 6-9) while the periphery area is deplete of the second oxide between its adjacent polysilicon lines (p. 7, ll. 9-11). Furthermore, a single implantation step occurs between adjacent polysilicon lines in the core area – after the first spacer etch, but before formation of the second spacer (oxide layer). (p. 7, ll. 1-2).

## VI. Statement of the Issues (37 C.F.R. § 1.192(c)(6))

A. Whether claims 1, 2, and 5-14 are unpatentable under 35 U.S.C. §102(e) as being anticipated by Nakajima *et al.* (U.S. 5,329,482).

## VII. Grouping of Claims (37 C.F.R. § 1.192(c)(7))

For the purposes of this appeal only, the claims are grouped as follows:

Claims 1, 2, and 5-14 stand or fall together.

## VIII. Argument (37 C.F.R. § 1.192(c)(8))

### A. Rejection of Claims 1, 2, and 5-14 Under 35 U.S.C. §102(e)

Claims 1, 2, and 5-14 are rejected under 35 U.S.C. §102(e) as being anticipated by Nakajima *et al.* (U.S. 5,329,482). Reversal of the rejection is respectfully requested for at least the following reasons.

#### i. Nakajima, *et al.* does not disclose each and every element recited in the respective claims.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). That is, the identical invention must be shown in as complete detail as is contained in the ... claim. *See Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner continues to assert that Nakajima *et al.* discloses "forming source and drain regions of MOS transistors of a memory cell section and a peripheral circuit section formed on one and the same substrate (Column 2, lines 66-67, and Column 3, lines 20-23, 38-41), therefore achieving doping of adjacent polysilicon lines in the same area, adjacent polysilicon lines with space between them and polysilicon lines in the core area and in the peripheral area." (Paper no. 15, p. 2). For additional support of her argument, the Examiner cites to Column 1, lines 29-33 and 41-43, for the assertion that "plural memory cells and peripheral circuit formation is recited for accessing the memory cells which is a disclosure of plural FETs in the

peripheral area." Applicants respectfully disagree.

Applicants submit that the Examiner has apparently misinterpreted the cited portions of Nakajima *et al.* by unduly broadening or altering the scope of its teachings.

In the first instance (cited portions in columns 2 and 3), Nakajima *et al.* discloses that a (single) MOS transistor can be formed in each of the memory cell section and the peripheral circuit section as shown in Nakajima's Fig. 5. Contrary to the Examiner's assertions, Nakajima *et al.* fails to disclose, teach or suggest depositing a first oxide layer over at least ***two adjacent polysilicon lines in each of a core area and a periphery area***...implanting an area located between at *least two adjacent polysilicon lines in the core area*...the core area retaining an amount of the second oxide *between the adjacent polysilicon lines* while the periphery area is deplete of the second oxide *between its adjacent polysilicon lines* – as claimed in the subject application. On its face, Nakajima *et al.* does not teach each and every element as claimed and recited herein.

The claimed invention relates to a method of fabricating dual insulating spacers located adjacent to plural polysilicon lines in each of a nonvolatile memory cell and its peripheral circuitry. Claim 1 of the present invention recites depositing a first oxide layer over at least *two adjacent polysilicon lines in each of a core area and a periphery area*...implanting an area located between at *least two adjacent polysilicon lines in the core area*...the core area retaining an amount of the second oxide *between the adjacent polysilicon lines* while the periphery area is deplete of the second oxide *between its adjacent polysilicon lines*. Independent claims 5 and 13 recite similar limitations. It is clear from the specification of the present invention that "area" is intended to mean two distinct locations: *the core area and the periphery area*. *See, e.g.*, page 1, line 10. Furthermore, independent claim 1 requires a single implantation step, which occurs *between adjacent polysilicon lines in the core area*, after the first spacer etch, but before formation of the second spacer (oxide layer).

Hence, on its face, Nakajima *et al.* plainly does not disclose ***each and every element*** of the claimed invention. Furthermore, Figure 5 of Nakajima *et al.* explicitly shows a single polysilicon line in a core area and a single polysilicon line in a peripheral area. Put another way,

these single polysilicon lines are in each of a core region and a peripheral circuit region. In fact, the core region is isolated or delimited from the peripheral region. *See* Column 5, lines 12-19. Thus, it is clear that the two lines are NOT in the same area according to the teachings of Nakajima, but rather are expressly described as being in two separate and distinct regions/areas of the substrate.

Since Nakajima *et al.* fails to teach adjacent polysilicon lines in the same area, it necessarily fails to disclose doping of adjacent polysilicon lines in the same area. The forming of source and drain regions *via* doping of regions surrounding a gate merely creates a gradient to effect potential current flow from the source to the drain. Thus, Nakajima *et al.*'s disclosure of *doping both sides of a single polysilicon line* is distinguishable and different from doping *between* adjacent polysilicon lines in the same area in order to form sources and drains.

In the second instance (referring to the Examiner's cited portions of column 1), Nakajima's disclosure that "a memory section consisting in a matrix array of a large number of memory cells and a peripheral circuit section for controlling data input and output ..." does not teach and/or anticipate depositing a first oxide layer over at least ***two*** *adjacent polysilicon lines in each of a core area and a periphery area*...implanting an area located between at *least two adjacent polysilicon lines in the core area*...the core area retaining an amount of the second oxide *between the adjacent polysilicon lines* while the periphery area is deplete of the second oxide *between its adjacent polysilicon lines* – as claimed in the subject application. Again, Applicants respectfully contend that the Examiner is unduly broadening or altering the scope of Nakajima *et al.* The cited portions of column 1 as well as of columns 2 and 3, or any other portion of Nakajima *et al.* plainly do not teach each and every element of the claimed invention.

Furthermore, in the Final Office Action (Paper no. 13), the Examiner appeared to contend and appears to maintain that forming source and drain regions of MOS transistors of a memory cell section (core) and a peripheral circuit section (periphery) on one and the same substrate achieves doping of adjacent polysilicon lines in the same area, adjacent polysilicon lines with space between them and polysilicon lines in the core area and in the peripheral area, and thus anticipates the present invention. Applicants' respectfully disagree.

According to the teachings of Nakajima *et al.* and the Examiner's own argument (*see* Paper no. 13), two separate regions/areas are formed on the Nakajima *et al.* substrate: a memory cell section and a peripheral circuit region. Thus, these two separate regions are not equivalent and cannot be considered as one. Instead, each is defined by independent characteristics and properties as reflected by at least their two different names, features, and locations on the substrate.

Moreover, it would be highly improper to assert that the memory cell section constitutes the same area as the peripheral circuit region or vice versa. More specifically, it would be highly improper to argue that a single polysilicon line is formed in both the memory cell region (core) and in the peripheral circuit region when such is not disclosed in Nakajima *et al.* Nakajima *et al.* teaches forming a single polysilicon line in the core and a single polysilicon line in the peripheral region. Contrary to the implications of the Examiner, these two regions located on one and the same substrate constitute distinct areas of the substrate.

Because Nakajima *et al.* fails to teach each and every element of the present invention, the subject application is not anticipated by Nakajima *et al.* Accordingly, this rejection should be reversed.

## IX. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited reference. Accordingly, it is respectfully requested that the rejections of claims 1, 2, and 5-14 be reversed. If any additional fees are due in connection with this document, the Commissioner if authorized to charge those fees to Deposit Account No. 50-1063.

Respectfully submitted,
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## X. Appendix of Claims (37 C.F.R. § 1.192(c)(9))

1. A method for forming a spacer, comprising:

depositing a first oxide layer over at least two adjacent polysilicon lines in each of a core area and a periphery area;

performing a first spacer etch in the core area and the periphery area;

implanting an area located between at least two adjacent polysilicon lines in the core area;

applying a second oxide layer over the core area and the periphery area; and

performing a second spacer etch over the periphery area, the core area retaining an amount of the second oxide between the adjacent polysilicon lines while the periphery area is deplete of the second oxide between its adjacent polysilicon lines.

2. The method of claim 1 wherein the first oxide layer has a thickness of less than one-half the distance between adjacent polysilicon lines.

5. A process for fabricating a non-volatile memory device comprising:

providing a substrate having a core area, a periphery area, and at least two adjacent polysilicon lines in each of the core area and the periphery area;

depositing a first oxide layer over the adjacent polysilicon lines;

performing a first spacer etch in the core area and the periphery area;

implanting an area located between at least two adjacent polysilicon lines in the core area;

depositing a second oxide layer over the core area and the periphery area; and

performing a second spacer etch over the periphery area.

6. The process of claim 5, wherein the first oxide layer has a thickness of less than one-half the distance between adjacent polysilicon lines.

7. The process of claim 5 further comprising performing a second spacer etch over the core area.

8. The process of claim 5, wherein the implanting of an area occurs after the performing of the first spacer etch.

9. The process of claim 5, further comprising implanting an area located between at least two polysilicon lines in the periphery area.

10. The process of claim 9, wherein the implanting of an area located between at least two polysilicon lines in the periphery area occurs after the performing of the first spacer etch.

11. The process of claim 9, wherein the implanting of an area located between at least two polysilicon lines in the core area occurs after the performing of the second spacer etch.

12. A process for making an electronic component comprising:

forming a memory cell by the process of claim 5; and

forming the electronic component comprising the memory cell.

13. A process for fabricating a memory cell comprising the steps of:

providing a substrate having a core area, a periphery area, at least two adjacent polysilicon lines in each of the core area and the periphery area, and first spacers adjacent at least two adjacent polysilicon lines in each of the core area and the periphery area; and

forming a second spacer adjacent at least one first spacer.

14. The process of claim 13, further comprising implanting an area located between at least two polysilicon lines in the core area.